

Digital ASIC Chip Designer

Responsibilities:

Primary responsibility is to participate in the development of high complexity, multi-core digital processor array chips for standard 0.18 μ CMOS technology, and for a novel 3 layer 0.15 μ FDSOI CMOS process. These chips will be based on synthesized digital circuits and will incorporate several design elements from successful previous vision chip designs relying on M/SIMD architectures.

The Candidate should be able to develop, analyze and verify the Verilog code description of the designs; furthermore, to organize and supervise the various stages of the ASIC design flow, including architecture determination, logic design and synthesis (with memory design), functional and timing verification, and initial post-silicon testing.

The specific responsibilities will/might include:

- Developing ASIC specification, architecture, and micro-architecture for a well-defined class of signal processing and communications algorithms
- Bit-exact MATLAB and/or C/C++ system modeling and simulation
- Development/simulation of RTL hardware implementations in Verilog
- Emulation of design elements on FPGA platforms
- Synthesis, gate level simulation, timing analysis, design for test
- Lab testing and debug of ASICs and complete consumer products
- Documentation/application note development and customer support

Experience:

Candidate must have MS-EE degree or equivalent and at least 5 years of relevant experience.

Skills required:

- Candidate must be hands-on experience in Verilog design and verification, and should have organization and supervision skills to be able to conduct a complete chip development cycle.
- Experience with emulation of ASIC designs in FPGAs
- Experience with ASIC design tools, timing closure, scan chain insertion
- Good documentation skills regarding code commenting and engineering specifications

Skills desirable:

- Data path arithmetic and RAM design experience.

- Experience with CMOS imagers and digital design for image processing chips
- Experience in mixed Verilog/VHDL designs
- Experience working with mixed-signal designers, taking part in SoC designs

Knowledge of tools:

CADENCE tools (with emphasis on Encounter product family), MentorGraphics ModelSim , Aldec Active-HDL.

Travel:

Travel will be required to synchronize development activities with our affiliate company in Central Europe (Hungary).

Compensation:

Compensation includes competitive salary and benefit package including general health, dental and vision care.

Company Information:

Eutecus Inc is located in Berkeley, CA with a proven track record in intelligent, high-speed imaging for industrial and military applications (see www.eutecus.com).

Eutecus Inc (located in Berkeley, CA) develops and delivers firmware and software capabilities in the area of improved high-speed image flow analytics for commercial and military applications. The core IP of the Company is based on its proprietary Cellular Visual Technology (CVT) enabling real time, bio-inspired and massively parallel visual computing. Mimicking the architecture and operations of the human eye, CVT yields significant improvements beyond the current state of the art in applications primarily in the areas of Security, Surveillance and Reconnaissance. Products delivered by Eutecus combine complex analytics with multi/many-core processor architectures and create massively parallel, configurable video processors for DSPs, FPGAs and ASICs targeted at a variety of OEM products and applications. Customers will benefit from CVT by simultaneously increasing the intelligence of embedded solutions while reducing their size, weight and power (see www.eutecus.com).

Respond in confidence to:

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