



Multi-core Video Analytics Engine

Embedded Video Analytics solution in Spartan-3A DSP FPGAs



Introduction

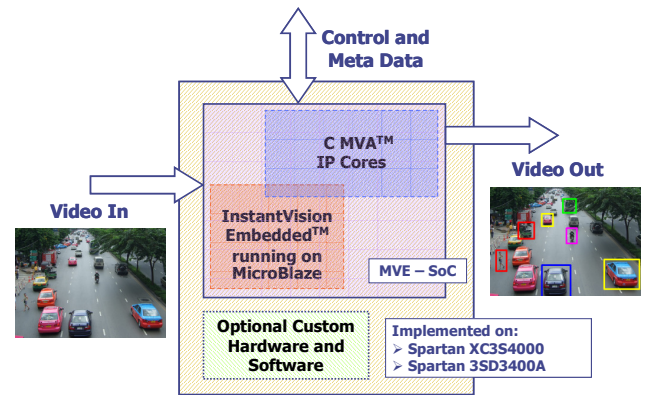
Multi-core Video Analytics Engine (MVE™) is an easily configurable, compact, high-performance processing architecture that can be used to implement complete video analytics solutions in a single FPGA embedded in intelligent surveillance cameras.

MVE combines an inherently parallel multi-core processing architecture, and embedded complex video analytics algorithms in a configurable building block, simplifying hardware design and programming effort resulting in reduced development cost and time to market.

Embedded solutions also benefit from low-cost and low-power implementation when embedding the entire MVE into a single FPGA. This initial commercial implementation of MVE is on the Xilinx Spartan-3A DSP 3400A FPGA chip.

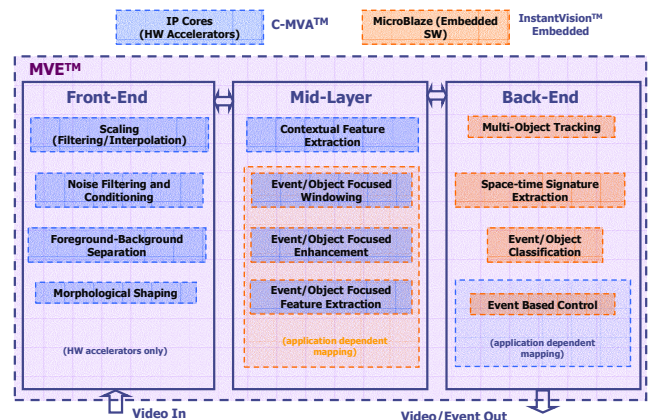
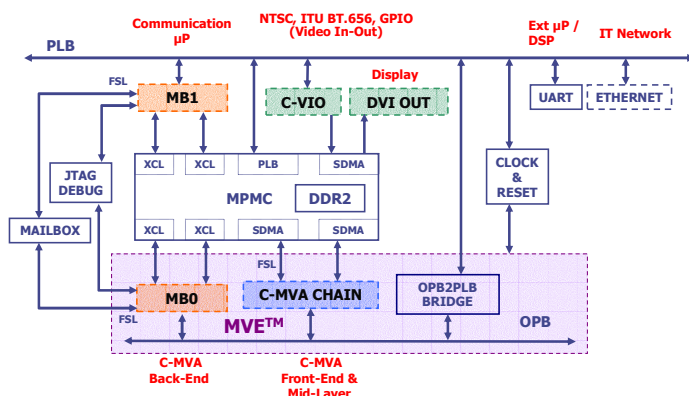
Implementation Statistics

The MVE™ is implemented in Xilinx Spartan-3A DSP 3400A FPGA within a SoC reference design with all required I/O functions for communication and data streaming (see block diagram). The entire SoC solution uses 91% of the logic slices, 81% of the block RAMs and 32% of the DSP slices. The MVE™ analytics engine (excluding the MPMC-PLB part of the backbone and specialized I/O components) utilizes only 46% of the logic slices, 44% of the block RAMs and 23% of the DSP slices.



Key MVE Features

- Stand-alone configurable Video Analytics engine based on high-performance C-MVA™ processor architecture
- Fully configurable VA functions such as people counting, detection of abandoned/stolen objects, entering forbidden zone, loitering, movement in wrong direction
- Enables single-chip VA solution in Xilinx FPGAs
- Image capture and video analysis done in HD image resolution at 30 frames per second
- Arbitrary number of events detected in parallel
- Pixel processing and acceleration implemented by parallel IP cores



www.eutecus.com/mve

On the reverse side:

MVE IP Core Information

Integrating MVE into your camera

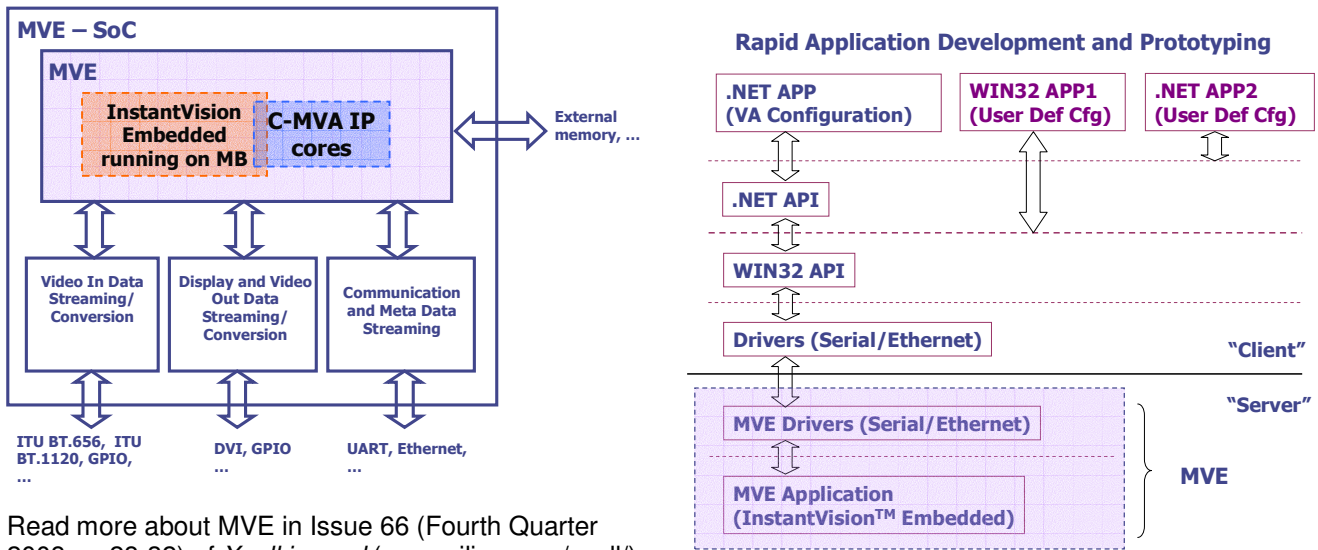
MVE IP Core Information

on Xilinx XtremeDSP Video Starter Kit (VSK) Spartan-3A DSP Edition

Core format	EDIF netlist, VHDL instantiation template, MicroBlaze or PPC libraries
Principal (algorithmic) modules	Image flow scaling and windowing, Statistical analysis, Image flow conditioning and noise filtering, Foreground-background separation, Binary morphological filtering, Signature and feature extraction, Multi-target tracking, Signature/feature analysis and event detection/classification
Digital video formats supported	4:4:4 YCrCb (24-bit) & 4:4:4 RGB (24-bit) Bayer pattern (Directly from sensor) Monochrome (8-bit)
Synchronization	Auto-synchronized to the incoming video flow
Video input standards	SDTV, HDTV (720p, 768p, 1080i, 1080p)
Supported input frame resolution	Any up to 4096x4096
Processed frame resolution	Unlimited line count by up to 1024 pixels/line For larger resolution windowing and/or downscaling could be used
Pipeline delay	2 video frames
External memory	Min. 1 input frame + (processed frame size) x 2 bytes + 4 Mbytes program & data storage
Parameter control	RS232 serial, Ethernet The core is fully programmable via PC GUI Ethernet connection is under development.

Implementing MVE in OEM Security Cameras

Next-generation MVE SoC embedded in your camera design



Read more about MVE in Issue 66 (Fourth Quarter 2008, pp28-32) of *Xcell journal* (www.xilinx.com/xcell/).

Eutecus develops and delivers firmware and software capabilities in the area of improved high-speed image flow analytics for commercial and military applications. The core IP of the Company is based on its proprietary Cellular Visual Technology (CVT™) enabling real time, bio-inspired and massively parallel visual computing. Mimicking the operation of the human eye, CVT yields significant improvements beyond the current state of the art in applications primarily in the areas of Security, Surveillance and Reconnaissance.

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